

TABLE II
LARGE-SIGNAL PERFORMANCES OF 60 μm EMITTER PERIPHERY n-p-n
AND p-n-p HBT'S AT 10 GHz

Device Type	Operation Mode	Output Power (mW)	Power Density (W/mm)	Gain (dB)	Power Added Efficiency
n-p-n	CW	120	2.0	6	40%
n-p-n	Pulsed	300	5.0	8	50%
p-n-p	CW	70	1.15	4	21%
p-n-p	Pulsed	120	2.0	5	25%

tered in p-n-p devices. Since this resistor is on the output side of the device, it has a significant effect on the power performance. A reduction in this parasitic resistor is necessary for improving power output and can be accomplished by the use of thicker subcollector layers and lower resistivity ohmic contacts.

IV. CONCLUSIONS

Microwave performances of n-p-n and p-n-p AlGaAs/GaAs HBT's with 100-nm-thick bases were compared. Although the small-signal characteristics were found to be similar, the power output capability of p-n-p devices was about half that obtained from n-p-n devices. Further optimization of the p-n-p structure, especially the subcollector layer, will probably result in devices comparable in performance. The availability of high-performance n-p-n and p-n-p HBT's will make it possible to implement complementary microwave and high-speed digital circuits.

ACKNOWLEDGMENT

The authors would like to thank T. Session, R. B. Smith, and M. K. Rector for technical assistance and W. R. Wisseman and D. N. McQuiddy, Jr., for support and encouragement.

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GaAs Power MESFET Performance Sensitivity to Profile and Process Parameter Variations

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Abstract—Large-signal performance sensitivities are calculated and compared for power GaAs MESFET's fabricated with uniform, ion-implanted, and lo-hi-lo conducting channel doping profiles. The large-signal sensitivities of the RF power and power-added efficiency are determined for the device designs as a function of variations in various process-dependent parameters. It is demonstrated that the channel doping profile design and breakdown voltage have the most significant influence upon large-signal RF performance.

I. INTRODUCTION

The rapid development of the state of the art in monolithic microwave integrated circuits has intensified the need to develop sophisticated CAD tools for use in circuit and device design. There is a particular need for large-signal device models capable of describing the nonlinear characteristics of active devices at microwave frequencies. In order to obtain the maximum benefit from a device simulator, the device model should be capable of describing the performance of a device before fabrication. In this manner much time, effort, and expense would be saved since device optimization studies could be performed before the device were actually fabricated. This consideration indicates a physics-based model, and the need to simulate RF operation indicates an analytic approach. Most of the large-signal device models presented to date, however, are based upon equivalent circuit techniques and require that the device be fabricated and characterized before the equivalent circuit is established. Since device characterization is, at best, an inexact process [1], the accuracy of the equivalent circuit techniques is not well established.

A physics-based, analytic large-signal GaAs MESFET model suitable for RF applications has recently been reported [2]. In this paper this model is used to investigate the large-signal RF performance sensitivities of GaAs power MESFET's to various device design and process-dependent parameters. The RF performances of power FET's with uniform, ion-implanted, and lo-hi-lo (buried channel) doping profile designs are considered and compared.

II. DEVICE MODEL

The device model used in this work [2] is based upon efficient solutions to the basic semiconductor device equations. The model solves a simplified form of the device equations analytically in

Manuscript received April 7, 1988; revised July 25, 1988. This work was supported in part by an Army Research Office Fellowship to D. E. Stoneking. The authors are with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695-7911.
IEEE Log Number 8824169.

TABLE I
PERFORMANCE SENSITIVITIES OF UNIFORMLY DOPED CHANNEL DEVICE
 $V_{ds} = 7 \text{ V}$, $I_{ds} = I_{dss}/2$

Variable	Nominal Value	(PAE) _{max} Sensitivity	P _{dB} Sensitivity
Gate Length (μm)	0.42	-0.20	-0.14
Channel thickness (μm)	0.30	-1.02	0.12
Saturation velocity (cm/s)	1.547	0.32	0.12
Low field mobility ($\text{cm}^2/\text{V s}$)	4000	0.05	-0.12
n channel	1.0d17	-0.38	-0.10
Breakdown voltage (V)	22	0.0	0.0
Gate drain breakdown resistance (Ω)	2	-0.8	0.0
Gate source leakage resistance (Ω)	2	0.0	0.0
Source resistance (Ω)	0.62	-0.03	-0.01
Source inductance (nH)	0.02	0.01	0.01
Drain resistance (Ω)	1.83	-0.07	-0.02
Drain inductance (nH)	0.05	+0.02	0.0
Gate resistance (Ω)	0.573	-0.01	0.01
Gate inductance (nH)	0.05	-0.01	0.0
Gate bias voltage (V)	-3.96	-1.12	-0.01
Drain bias voltage (V)	6.94	-0.11	-0.21

TABLE II
PERFORMANCE SENSITIVITIES OF ION-IMPLANTED PROFILE DEVICE
 $V_{ds} = 7 \text{ V}$, $I_{ds} = I_{dss}/2$

Variable	Nominal Value	(PAE) _{max} Sensitivity	P _{dB} Sensitivity
Gate Length (μm)	0.42	-0.21	-0.08
Channel thickness (μm)	0.35	-0.08	-0.02
Saturation velocity (cm/s)	1.5x10 ⁷	0.53	0.02
Low field mobility ($\text{cm}^2/\text{V s}$)	4000	0.05	0.01
Peak doping (cm^{-3})	1.8x10 ¹⁷	0.04	0.03
Breakdown voltage (V)	19.4	0.0	0.0
Gate drain breakdown resistance (Ω)	2.0	0.0	0.0
Gate source leakage resistance (Ω)	2.0	0.04	0.0
Source resistance (Ω)	0.62	0.05	0.02
Source inductance (nH)	0.02	0.04	0.0
Drain resistance (Ω)	1.83	-0.50	0.07
Drain inductance (nH)	0.05	0.04	0.3
Gate resistance (Ω)	0.573	0.04	0.0
Gate inductance (nH)	0.05	0.04	0.01
Gate bias voltage (V)	-1.804	2.80	-0.80
Drain bias voltage (V)	6.94	-1.73	-0.28

the time domain. The device conduction and displacement currents are calculated as a function of applied terminal dc and RF voltages. The model is suitable for both transient and RF analyses. For RF investigations the time-domain device model is interfaced with a frequency-domain linear circuit simulator by means of the harmonic balance technique [3], [4]. Since the resulting simulator includes the device/circuit interface, the simulator is suitable for performance and optimization investigations of both the device and the circuit.

The model accepts as input data (1) device information such as geometry, doping profile, and bias conditions and (2) circuit information such as microwave circuit topology and RF drive information. The circuit information is supplied by means of linear impedance matrices that are determined for a given circuit topology from standard linear microwave simulators. The complete simulator returns information such as RF output power, power-added efficiency, gain, input/output impedances, and spectrum information. The model is capable of investigating the RF performance of a GaAs MESFET as a function of device design parameters without the need to first fabricate and characterize the device. The model has previously been used to investigate a C-band monolithic power amplifier [5] and the parameter sensitivities of ion-implanted power FET's [6]. Excellent agreement between model predictions and experimental data is obtained.

TABLE III
PERFORMANCE SENSITIVITIES OF LO-HI-LO DOPED CHANNEL DEVICE
 $V_{ds} = 7 \text{ V}$, $I_{ds} = I_{dss}/2$

Variable	Nominal Value	(PAE) _{max} Sensitivity	P _{dB} Sensitivity
Gate Length (μm)	0.42	-0.61	-0.06
Channel thickness (μm)	0.35	-0.24	-0.02
Saturation velocity (cm/s)	1.5x10 ⁷	0.17	0.00
Low field mobility ($\text{cm}^2/\text{V s}$)	4000	-0.51	0.00
Breakdown voltage (V)	31.0	0.0	0.0
Gate drain breakdown resistance (Ω)	2.0	0.0	0.0
Gate source leakage resistance (Ω)	2.0	0.0	0.0
Source resistance (Ω)	0.62	-0.03	0.0
Source inductance (nH)	0.02	0.02	0.0
Drain resistance (Ω)	1.83	-0.08	-0.02
Drain inductance (nH)	0.05	0.03	0.02
Gate resistance (Ω)	0.573	-0.01	-0.01
Gate inductance (nH)	0.05	0.0	0.0
Gate bias voltage (V)	-3.806	-0.48	-0.01
Drain bias voltage (V)	6.94	-0.06	0.28
n low (μm^{-3})	0.12	-0.72	0.46
n high (μm^{-3})	0.065	-0.82	0.14
n low (cm^{-3})	5.0x10 ¹⁶	-0.02	0.0
n high (cm^{-3})	5.0x10 ¹⁷	-0.61	-0.06

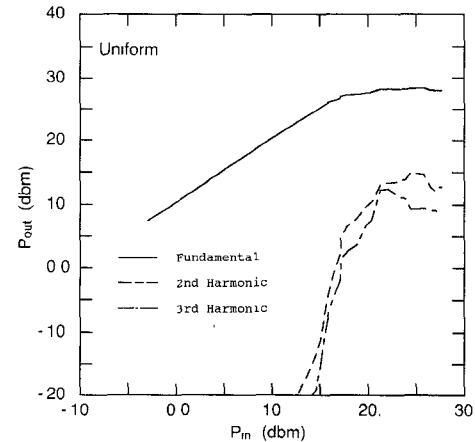


Fig. 1. RF power output versus power input for the uniform doped channel device ($V_{ds} = 7 \text{ V}$, $I_{ds} = I_{dss}/2$, $F = 10 \text{ GHz}$).

III. RF PERFORMANCE COMPARISON

The three device doping profiles that were considered in this work consist of uniformly doped, ion-implanted, and lo-hi-lo (buried channel) designs. Channel doping details are indicated in Tables I, II, and III. Each profile type was optimized to produce a maximum power-added efficiency (PAE) at 10 GHz with a bias of $V_{ds} = 7 \text{ V}$ and $I_{ds} = I_{dss}/2$. All devices had nominal gate lengths of $0.5 \mu\text{m}$ and gate widths of 1 mm .

The RF output power versus input power characteristics for the three devices when operated in a common-source amplifier configuration with 50Ω source and load impedances are shown in Figs. 1, 2, and 3. Also shown is the output power at the second and third harmonics. The uniformly doped and lo-hi-lo profile devices produce similar output power and both devices produced about 1 dB lower linear power than the ion-implanted device, but about 2 dB greater saturated power. The ion-implanted device saturated at a slightly lower input power than the other two devices. The harmonic output powers from the uniform and lo-hi-lo devices were significantly less than that from the ion-implanted device. Since harmonic power is an indicator of non-linear operation, this suggests that ion-implanted devices should produce the least linear operating range and the most limited

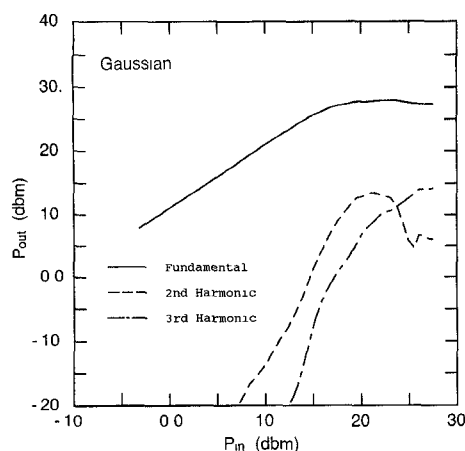


Fig. 2. RF power output versus power input for the ion-implanted profile device ($V_{ds} = 7$ V, $I_{ds} = I_{dss}/2$, $F = 10$ GHz).

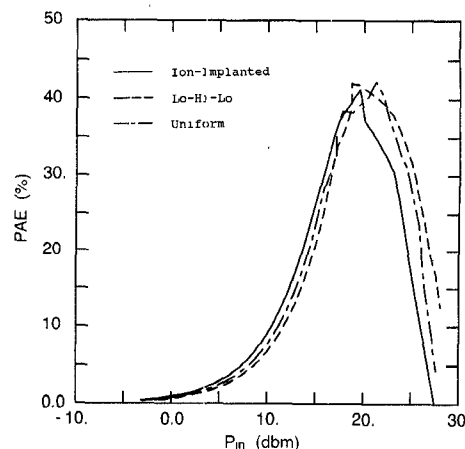


Fig. 4. Power-added efficiency versus input power for the three devices.

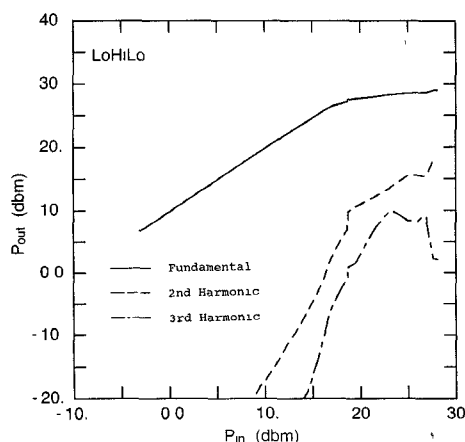


Fig. 3. RF power output versus power input for the lo-hi-lo profile device ($V_{ds} = 7$ V, $I_{ds} = I_{dss}/2$, $F = 10$ GHz).

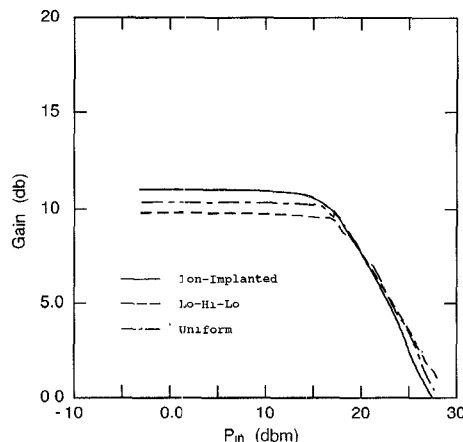


Fig. 5. Gain versus input power for the three devices.

dynamic range. The lo-hi-lo device, in particular, appears well suited for linear, high dynamic range applications.

The PAE and gain characteristics for the three devices are shown in Figs. 4 and 5. All three devices are capable of generating essentially the same maximum PAE (about 43 percent). The uniform and lo-hi-lo devices, however, produce near maximum PAE over a larger range of P_{in} than the ion-implanted device, while the PAE characteristic for the ion-implanted device is shifted toward lower values of P_{in} . The ion-implanted device produces the greatest linear gain (about 11 dB) and the lo-hi-lo device produces the smallest linear gain (about 9.5 dB). The ion-implanted device saturates at an input power approximately 2 dBm before the other two devices. Once saturation is achieved, the ion-implanted device produces approximately 1 to 2 dB less gain than the other devices at a given input power level. The lo-hi-lo device produces the greatest saturated gain.

IV. PERFORMANCE SENSITIVITY STUDY

The performance sensitivities of the 1 dB compressed power ($P_{1\text{ dB}}$) and PAE were calculated for each device for variations in various design and process parameters. Each design parameter of interest was varied about its nominal value, and the relative sensitivity of the RF performance parameter was calculated. The

performance sensitivities are defined as normalized small-signal variations about the nominal parameter value [6].

The RF performance sensitivities for the three devices are shown in Tables I, II, and III. As indicated in the tables, both the PAE and the $P_{1\text{ dB}}$ for all three devices are most sensitive to the conducting channel design under the gate. This indicates that tight tolerance must be maintained on the conducting channel design if optimum and repeatable performance is to be obtained. For example, in order for the uniform doped device to maintain a PAE greater than 40 percent, the channel thickness must be within 12 percent of the design value. For thick channels the gate is not able to exercise optimum control over the channel current and, therefore, output power and PAE degrade. For thin channels the channel current is reduced, which also degrades output power and PAE . For this same device the PAE is above about 40 percent for approximately a 20 percent variation in the channel doping density.

Although the data presented in the tables do not indicate sensitivity to gate-drain breakdown voltage, the magnitude of the breakdown voltage and the dc operating point must be considered. As the breakdown voltage is reduced, significant increases in RF performance sensitivity are observed. For example, the PAE 's for the three devices biased at 7 V are shown in Fig. 6 as a function of gate-drain breakdown voltage. The ion-

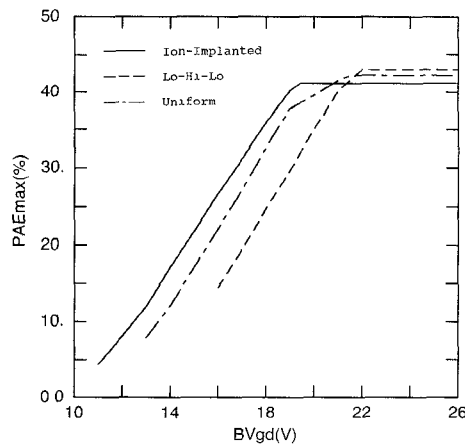


Fig. 6 Maximum power-added efficiency versus gate-drain breakdown voltage for the three devices ($V_{ds} = 7$ V, $I_{ds} = I_{dss}/2$, $F = 10$ GHz)

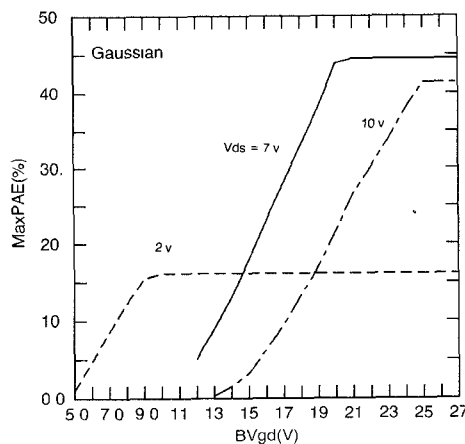


Fig. 7 Maximum power-added efficiency versus gate-drain breakdown voltage for the ion-implanted device for three different drain bias voltages.

implanted device is able to tolerate the lowest breakdown voltage before significant degradation in PAE occurs. Reducing the breakdown voltage below approximately 19 V for the ion-implanted device, 21 V for the uniform device, and 22 V for the lo-hi-lo device produces significant degradation in RF performance. The dependence of PAE upon BV_{gd} for the ion-implanted device is shown in Fig. 7. Data are shown for three drain bias voltages with the drain current equal to one half I_{dss} . The PAE degrades rapidly for BV_{gd} less than 25 V for $V_{ds} = 10$ V, 20 V for $V_{ds} = 7$ V, and 9 V for $V_{ds} = 2$ V. Higher breakdown voltages allow larger RF voltages to be applied before waveform clipping and RF performance degradation occur.

V. CONCLUSIONS

The RF large-signal performance sensitivities for GaAs MESFET's with uniformly doped, ion-implanted, and lo-hi-lo doping profiles have been investigated. All three device designs are capable of generating PAE in excess of 40 percent at 10 GHz. Optimized lo-hi-lo and uniform profile devices appear to produce the greatest saturated RF output power and gain and the most linear response. Ion-implanted devices produce the greatest linear gain, but have the least saturated RF power and gain and the most limited dynamic range. The RF performance of the

devices is most sensitive to the conducting channel design and the gate-drain breakdown voltage when the breakdown voltages are relatively low.

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De-embedding Coplanar Probes with Planar Distributed Standards

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Abstract—Two methods are used to de-embed coplanar probes using offset coplanar waveguide shorts and transmission lines. The accuracy of the de-embedded measurements is verified. The S parameters of lumped standards provided by the manufacturer of the probes are measured and found to be suitable for purposes of calibration up to 26 GHz.

I. INTRODUCTION

Coplanar probes are widely used by manufacturers of microwave integrated circuits to characterize the S parameters of microwave transistors and monolithic integrated circuits (MMIC's). The probes introduce significant measurement errors which must be removed if transistor S parameters are to be accurately measured. A procedure referred to as "de-embedding" has been developed for this purpose [1], [2].

The coplanar probes are usually de-embedded by measuring the uncorrected S parameters of a set of lumped impedance "standards" provided by the manufacturer. A numerical algorithm is then used to determine the error coefficients of the measurement system from the uncorrected measurements of the impedance "standards." The accuracy to which the impedance of these "standards" are known limits the accuracy of the calibration procedure.

In this work, two different and independent sets of "standards" were utilized for de-embedding. These consisted of the coplanar waveguide (CPW) through lines and offset CPW shorts that were developed for de-embedding the Cascade Microtech type WPH-105-10 probe heads from 5 to 25 GHz. In each case, the accuracy of the calibration was verified by measuring the S parameters of planar circuits not used in the de-embedding

Manuscript received April 8, 1988; revised July 5, 1988.

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IEEE Log Number 8824174